9. (Amended) A method of forming a transistor structure, comprising:

forming a transistor gate over a substrate, the transistor gate comprising a sidewall which comprises electrically conductive material;

forming an electrically insulative material along the electrically conductive material of the transistor gate sidewall; the electrically insulative material comprising at least two separate layers; a first of the at least two layers comprising Al_pO_q, wherein p and q are greater than 0 and less than 10; a second of the at least two layers consisting essentially of silicon and nitrogen;

anisotropically etching the electrically insulative material to form a spacer along the transistor gate sidewall; the anisotropically etching comprising etching both of the first and second of the at least two layers; and

wherein the first of the at least two layers is between the second of the at least two layers and the transistor gate sidewall.

13. (Amended) The method of claim 9 wherein the first of the at least two layers consists essentially of Al_pO_q.

32. (New) The method of claim 9 wherein the first of the at least two layers consists of Al_pO_q.

33. (New) The method of claim 9 wherein the first of the at least two layers consists of Al_2O_3.